In the specification:

Amend the paragraph on page 1, lines 10 to 21 as follows:

As transistor device densities continue to increase, minor fabrication and operational defects can ~~have~~ impact transistor operation inversely proportional to ~~with~~ the size of the transistor. One of the well-known problems for small field effect transistors is channel hot carrier effects. For example, when a conventional metal oxide semiconductor field effect transistor (MOSFET) structure is scaled down to one micron or less, the potential energy of an electron changes dramatically when it hits the n^+ drain boundaries. This sudden change in potential energy in a short distance tends to create a high electric field. This causes the electrons to behave differently within the semiconductor lattice. Electrons which have been activated by high electric fields are referred to as "hot electrons", and can, for example, penetrate into or through the gate dielectric. Electrons that penetrate into, but not through, the gate dielectric can cause the gate dielectrics to store charge over time, until the transistor ultimately fails.

Amend the paragraph on page 4, lines 11 to 19 as follows:

FIG. 1 depicts a schematic cross-sectional view of a transistor 10 in accordance with an aspect of the present invention. The transistor 10 can be a p-channel transistor or an n-channel transistor. For purposes of simplicity of explanation, the following discussion of FIG. 1 will assume an n-channel transistor, such as an NMOS. The transistor 10 includes a gate structure 12 that is disposed over a gate dielectric layer 14. To form the gate structure 12, a corresponding area is patterned and then later doped. The gate structure 12 can include a poly silicon gate (*e.g.*, polygate). The poly gate is doped to render it conductive, such as through diffusion or ~~of~~ ion implantation. The particular doping of the polygate may depend on the type of device (*e.g.*, whether it is an n-channel or p-channel device

Amend the paragraph at page 5, lines 15 to 25 as follows:

The floating region 24 can be formed by implanting suitable dopant at a lower dose than the dose of dopant utilized to form the LDD region 20. This provides for a shallower, lighter doped region within the LDD region 20. In the example of FIG. 1, the floating ring extends from at or near a surface of the substrate 26 to a depth that is less than the junction depth of the LDD region 20. By way of example, for an NMOS transistor, the floating region 24 can be implemented as boron (B_{11} or BF_2), as well as any other p-type dopant. The final ~~finial~~ doping level of the floating region 24 can be either P type or still n type with reduced concentration relative to the concentration of the LDD region 20. Formation of the source/drain regions 18 overpowers the lightly doped portions that are implanted with the floating region 24 due to higher doping level of the source/drain region that the floating region 24.

Amend the paragraph at page 7, lines 9 to 21 as follows:

FIG. 3 illustrates that a polysilicon gate (or polygate) 106 that can be formed over the dielectric layer 104. The polygate structure 106 can be formed via a series of deposition, patterning and etching steps. For example, one or more conductive layers are formed over the dielectric layer 104~~, such~~ using any suitable technique including CVD techniques, such as LPCVD or PECVD (*e.g.*, tetra-ethyl-ortho-silicate (TEOS)) followed by a reoxidation process. The polysilicon can be formed in a polycrystalline state or an amorphous state, which is later converted to a crystalline state. The polysilicon can also be formed using *in-situ* doping techniques and implantation techniques. The conductive layer is patterned and then etched (*e.g.*, plasma dry etching or other dry and/or wet etching techniques) to form the gate structure 106. Following etching and formation of the gate structure 106, the remaining patterned photoresist layer can be stripped (*e.g.*, Ultra-Violet (UV)/ Ozone (O_3)/ Sulfuric Acid (H_2SO_4) and the structure can be cleaned by any suitable cleanup process.